Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method, comprising:

   (a) measuring a skew between a data signal and a clock signal at a receiving ~~end~~ side of a serial link; and

   (b) adjusting a phase relationship between said data signal and said clock signal to reduce said skew, wherein said adjusting of said phase relationship occurs at a transmitting ~~end~~ side of said serial link.

2. (Canceled)

3. (Original) The method of claim 1 further comprising receiving said measured skew at a skew adjustment unit and determining said phase relationship before said adjusting a phase relationship.

4. (Original) The method of claim 1 further comprising programming said phase relationship into a semiconductor chip.

5. (Original) The method of claim 1 wherein said adjusting a phase relationship further comprises imposing a delay on at least one of said signals.

6. (Original) The method of claim 5 wherein said adjusting a phase relationship further comprises imposing a delay on both of said signals.

7. (Original) The method of claim 1 wherein said adjusting a phase relationship further comprises adjusting a phase offset between a pair of phasors associated with a pair of phase interpolators, a first of said phasors used to derive a second clock signal that times the transmission of said data signal, a second of said phasors used to derive said clock signal.

8. (Currently Amended) An apparatus, comprising:

(a) a ~~transmitting unit~~ transmitter coupled to a ~~receiving unit~~ receiver by a serial link, said serial link ~~configured~~ comprising a clock signal line and a data signal line to transport a clock signal and a data signal;

(b) ~~a~~ skew measurement ~~unit~~ circuitry coupled to said serial link, ~~such that said coupling of~~ said skew measurement ~~unit~~ circuitry coupled to said serial link ~~is~~ closer to said ~~receiving unit~~ receiver than said transmitter ~~transmitting unit~~, said skew measurement circuitry to measure a skew between said clock signal and said data signal; and

(c) ~~a~~ skew adjustment circuitry ~~unit~~ coupled to said skew measurement circuitry and said transmitter, said skew adjustment circuitry ~~transmitting unit~~ to adjust said skew at a transmitting ~~end~~ side of said serial link in response to a signal from said skew measurement circuitry~~unit~~.

9. (Currently Amended) The apparatus of claim 8 further comprising a programmable delay unit within said transmitter ~~transmitting unit~~, said programmable delay unit coupled to said skew adjustment circuitry~~unit~~, said programmable delay unit having an output node ~~corresponding~~ to provide one of said signals.

10. (Currently Amended) The apparatus of claim 8 further comprising a second programmable delay unit within said ~~transmitting unit~~transmitter, said second programmable delay unit coupled to said skew adjustment circuitry~~unit~~, said second programmable delay unit having an output node ~~corresponding~~to provide another of said signals.

11. (Original) The apparatus of claim 9 wherein said programmable delay unit further comprises a cascade of inverters.

12. (Original) The apparatus of claim 11 wherein each of said inverters within said cascade of inverters has an adjustable propagation delay.

13. (Currently Amended) The apparatus of claim 8 wherein transmission of said data signal is timed according to a phase interpolator output signal.

14. (Currently Amended) The apparatus of claim 8 wherein clock signal is derived from a phase interpolator output signal.

15. (Currently Amended) The apparatus of claim 14 wherein said phase interpolator further comprises a skew control input that adjusts a phasor phase offset, said skew control input coupled to said skew adjustment ~~unit~~circuitry.

16. (Currently Amended) The apparatus of claim 8 wherein said skew adjustment circuitry ~~unit~~ further comprises a CPU.

17. (Currently Amended) An apparatus, comprising:

(a) a network interface coupled to a transmitter~~transmitting unit~~;

(b) a ~~receiving unit~~ receiver coupled to said ~~transmitting unit~~ transmitter by a serial link, said serial link ~~configured~~ comprising a clock signal line and a data signal line to transport a clock signal and a data signal;

(c) ~~a~~ skew measurement ~~unit~~ circuitry coupled to said serial link ~~such that said coupling of said skew measurement unit to said serial link is~~ closer to said receiver ~~receiving unit~~ than said transmitter~~transmitting unit~~; and,

(d) ~~a~~ skew adjustment ~~unit~~ circuitry coupled to said skew measurement circuitry and said ~~transmitting unit~~ transmitter, said skew adjustment circuitry to adjust said skew at a transmitting ~~end~~ side of said serial link in response to a signal from said skew measurement circuitry~~unit~~.

18. (Original) The apparatus of claim 17 wherein transmission of said data signal is timed according to a phase interpolator output.

19. (Currently Amended) The apparatus of claim 17 wherein said clock signal is derived from a phase interpolator output.

20. (Currently Amended) The apparatus of claim 19 wherein said phase interpolator further comprises a skew control input ~~that~~ to adjust~~s~~ a phasor phase offset, said skew control input coupled to said skew adjustment circuitry~~unit~~.

21. (Original) The apparatus of claim 17 wherein said skew adjustment ~~unit~~ circuitry further comprises a CPU.

22. (Currently Amended) The apparatus of claim 17 wherein said ~~transmitting unit~~ transmitter further comprises a parallel to serial converter ~~that~~ to crafts said data signal, said parallel to serial converter coupled to ~~receiving parallel data from~~ said network interface to receive parallel data.

23. (Original) The apparatus of claim 17 wherein said network interface corresponds to a physical layer.

24. (Original) The apparatus of claim 17 wherein said network interface corresponds to a media access control layer.

25. (new) A semiconductor chip comprising:

a) a serial link transmitter comprising a serial clock signal output and a serial data signal output;

b) skew adjustment circuitry coupled to said serial link transmitter, said skew adjustment circuitry to adjust a skew between said serial clock signal and said serial data signal, said skew adjustment circuitry comprising an input node to receive an indication of said skew measured closer to said serial link's receiver than said serial link transmitter.

26. (new) The apparatus of claim 25 wherein said serial link transmitter comprises a programmable delay unit having an output node from which said serial link clock signal flows.

27. (new) The apparatus of claim 26 wherein said programmable delay unit comprises a cascade of inverters.

28. (new) The apparatus of claim 25 wherein said transmitter comprises a phase interpolator to time the transmission of said data signal.

29. (new) The apparatus of claim 15 wherein said transmitter comprises a phase interpolator to time the transmission of said clock signal.